STMicroelectronics
IPD - ASD & IPAD™ Division[1]
BU Rectifiers

(1) IPD: Industrial & Power Discretes - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PIL
Product/Process Information Letter

Internal wafer epitaxy process qualification for Power Schottky Silicon Carbides Diodes

Notification number:	IPD-DIS/15/9211	**Issue Date**	20/04/2015
Issued by	Aline AUGIS		

Product series affected by the change	
	STPSC1006D STPSC10H065B-TR STPSC10H065D STPSC10H065DI STPSC10H065DY STPSC10TH13TI STPSC1206D STPSC12C065DY STPSC12H065CT STPSC12H065D STPSC12H065DY STPSC16H065CT STPSC2006CW STPSC20H065CT STPSC20H065CTY STPSC20H065CW STPSC20H065CWY STPSC40065CW STPSC406B-TR STPSC406D STPSC4H065B-TR STPSC4H065D STPSC4H065DI STPSC606D STPSC606G-TR STPSC6H065B-TR STPSC6H065D STPSC6H065DI STPSC6H065G-TR STPSC6TH13TI STPSC806D STPSC806G-TR STPSC8H065B-TR STPSC8H065CT STPSC8H065D STPSC8H065DI STPSC8H065G-TR STPSC8TH13TI

Reason for change

STMicroelectronics is now going to implement the internal epitaxy process for its Power Schottky Silicon Carbides Diodes.

This process qualification is the result of the constant investments made by STMicroelectronics in the Silicon Carbides technology. It illustrates the commitment of the Company to reinforce its leading position in the Silicon Carbides market.

Thanks to this investment, STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction, especially as volumes grow.

Effects of change

No impact on the electrical parameters of the products, with reference to their datasheet. The verification is included in the qualification program.

Product identification and traceability

A QA number and an internal codification will be created to ensure the traceability.

Qualification complete date	W14-2015

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Power Schottky	Silicon Carbide	STPSC606D	Now
Power Schottky	Silicon Carbide	STPSC8H065D	Now

Change implementation schedule

Estimated production start	Estimated first shipments
Week 19-2015	**Week 30-2015**

Qualification:	QRP15020-Rev1 is attached

Comments:

Qualification Report

Internal wafer epitaxy process for Power Schottky Silicon Carbide diodes

General Information	
Product Line	*Rectifiers*
Product Description	*Silicon Carbide diodes*
Product Group	*IPG*
Product division	*ASD & IPAD*
Package	*Multiple*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST Catania (ITALY)*
EWS plat	*ST Catania* *ST Singapore*
Assembly plant	*ST Shenzhen (China)*
Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	10/04/2015	5	I. Ballon	JP Rebrassé	Initial qualification

Note: This report is a summary of the test trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47-H	Stress-Test-Driven Qualification of Integrated Circuits
AEC Q101	Stress test Qualification for Automotive Grade Discrete semiconductors

2 GLOSSARY

SS	Sample Size
EWS	Electrical Wafer Sorting
PC	Preconditioning
HTRB	High Temperature Reverse Bias
THB	Temperature Humidity Bias
TC	Temperature Cycling
IOLT	Intermittent Operating Life Test
RIFSM	Repetitive IFSM

3 EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the implementation of internal epitaxy process for Power Schottky Rectifiers Silicon Carbide Diodes and demonstrates it has no impact on products.
The involved products are listed in the table below:

Product sub-Family	Product devices
Silicon Carbide Power Schottky Rectifiers	All STPSCxxx except 1200V

The reliability test methodology used follows the JESD47-H and AEC-Q101: « Stress Test Driven Qualification Methodology ».
The following tests ensuing are:

- TC, IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB to check the robustness to corrosion and the good package hermeticity.
- Comparative parametric verification
- Comparative electrical yields verification

3.2 Conclusion

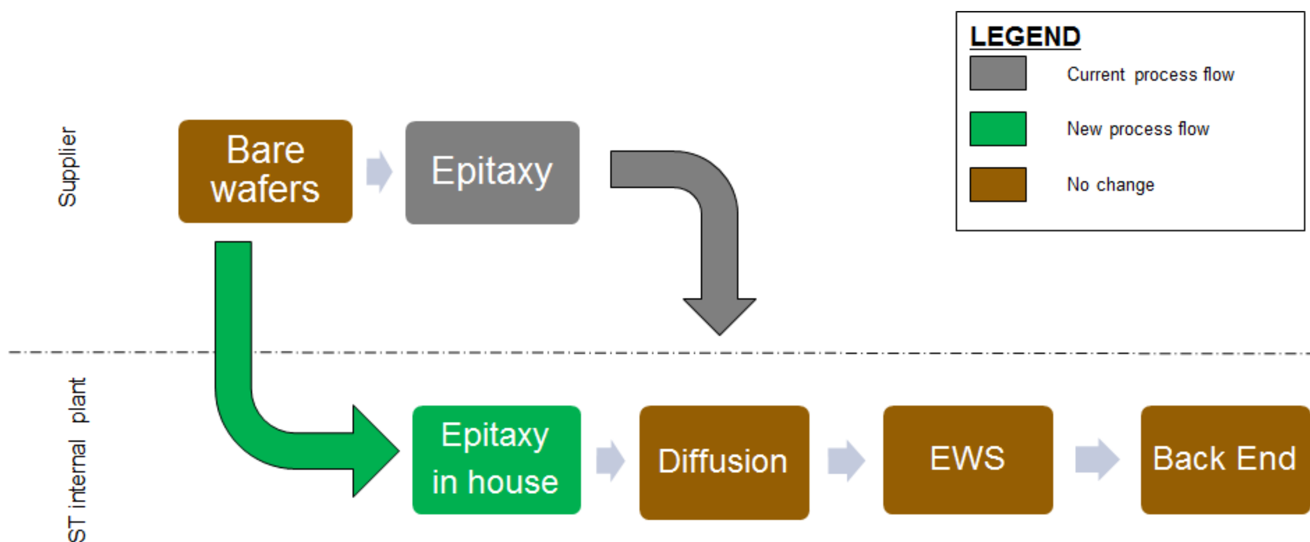
Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

The process key parameters comparison and the different tests have shown that there is no impact on electrical results of the products with the reference to their datasheet.

4 CHANGE DESCRIPTION

The epitaxy process will be performed in ST Italy Catania, keeping identical key process parameter. Moreover, there is no change in term of diffusion process, EWS process, Assembly process & Final Testing. There is consequently no impact on the electrical parameters.

Description	Current	New
Bare substrates	Substrate suppliers	Substrate suppliers
Epitaxy Fab	Substrate suppliers	Substrate suppliers or ST Italy Catania
Wafer Fab	ST Italy Catania	ST Italy Catania
EWS Area	ST Italy Catania ST Singapore Toa Payoh	ST Italy Catania ST Singapore Toa Payoh
Assembly and FT	ST Shenzhen	ST Shenzhen



5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Commercial Product	Comments
Lot 1	STPSC606D	Reference lot (Epitaxy at substrate supplier)
Lot 2		1st Qualification Lot (Epitaxy at ST wafer fab)
Lot 3		2nd Qualification Lot (Epitaxy at ST wafer fab)
Lot 4	Generic part in SiC 6A 650V in TO-220 package	Reference lot (Epitaxy at substrate supplier)
Lot 5		3rd Qualification Lot (Epitaxy at ST wafer fab)
Lot 6	Generic part in SiC 16A 650V in TO-220 package	Reference lot (Epitaxy at substrate supplier)
Lot 7		4th Qualification Lot (Epitaxy at ST wafer fab)

5.2 Test plan and results summary

Test	PC*	Std ref.	Conditions	SS	Steps	Failure/SS				Note
Die Oriented Tests										
						Lot 1 Reference	**Lot 2**	**Lot 3**	**Lot 5**	
HTRB	N	JESD22 A-108	Tj=150°C VR=0.8xVRRM	77	168 Hrs				0/77	
					500 Hrs				0/77	
					1000 Hrs				0/77	
Package Oriented Tests										
						Lot 1 Reference	**Lot 2**	**Lot 3**	**Lot 5**	
TC	N	JESD22 A-104	-65°C/+150°C 2cycles/hour	80 + 40 reference	500 cycles	0/40	0/40	0/40		
					1000 cycles	0/40	0/40	0/40		
						Lot 1 Reference	**Lot 2**	**Lot 3**	**Lot 5**	
THB	N	JESD22 A-101	85°C; 85%HR VR=100V	77	500 Hrs				0/77	
					1000 Hrs				0/77	

						Lot 1 Reference	Lot 2	Lot 3	Lot 5	
IOLT	N	Mil Std 750 method 1037	ΔTc = 85°C $t_{on} = t_{off}$ = 210s	77	4286cy		0/77			
					8572cy		0/77			

						Lot 1 Reference	Lot 2	Lot 3	Lot 5	
RIFSM	N	N/A	If peak = IFSM = 49A Ta = 25°C Pulse time = 10ms	24	100 hits				0/24	

5.3 Test Information

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
Repetitive IFSM	IFSM pulses at datasheet value are runs in repetitive mode (30sec off between 2 consecutive hits).	To test die and contacts integrity versus high temperature repetitive pulses

Comparative electrical parameters

STPSC606D Average values	Reference Lot 1	Lot 2
IR 25°C 600V (µA)	4	5
IR 150°C 600V (µA)	97	96
VF 25°C at I0=6A (V)	1.54	1.47
VF 150°C at I0=6A (V)	1.94	1.84
IFSM 25°C at 10ms (A)	29	31

Generic part in SiC 16A / 650V in TO-220 package Average values	Reference Lot 6	Lot 7
IR 25°C 650V (µA)	21	16
IR 150°C 650V (µA)	94	94
VF 25°C at I0=16A (V)	1.52	1.49
VF 150°C at I0=16A (V)	1.79	1.73
IFSM 25°C at 10ms (A)	144	150

Comparative measurements for datasheet parameters have revealed no significant difference.

Comparative electrical yields at Test area

STPSC606D	Reference Lot 1	Lot 2
T&F yield	97.1%	99.1%

Generic part in SiC 6A / 650V in TO-220 package	Reference Lot 4	Lot 5
T&F yield	96.4%	98.1%

Comparative yields have also proved to be fully correlated. It appears that no major difference has been raised. Final test remains unchanged.